ABSTRACT

[Abstract of the Disclosure]

A dual port semiconductor memory device, including PMOS scan transistors, is provided. The dual port semiconductor memory device includes two PMOS transistors, two NMOS pull-down transistors, two NMOS pass transistors, and a PMOS scan transistor. Since the scan transistor is a PMOS transistor, noise margins can be improved. In addition, these seven transistors are arranged in two n-wells and 2 p-wells, and these n-wells and p-wells are arranged in series in an alternating manner. Therefore, the length of a memory cell along the short axis of the memory cell is very short. This memory cell layout helps shorten the length of a bit line by arranging a pair of bitlines in parallel with well boundaries, i.e., in the direction of the short axis of the memory cell, and makes it possible to prevent crosstalk between a bitline and a complementary bitline that constitute a pair of bitlines by arranging conductive lines between the bitline and the complementary bitline.

[Representative Drawing]

FIG. 3

[Index Words]

SRAM, dual port, scan transistor, noise margins, bitline cross-talking